Figures

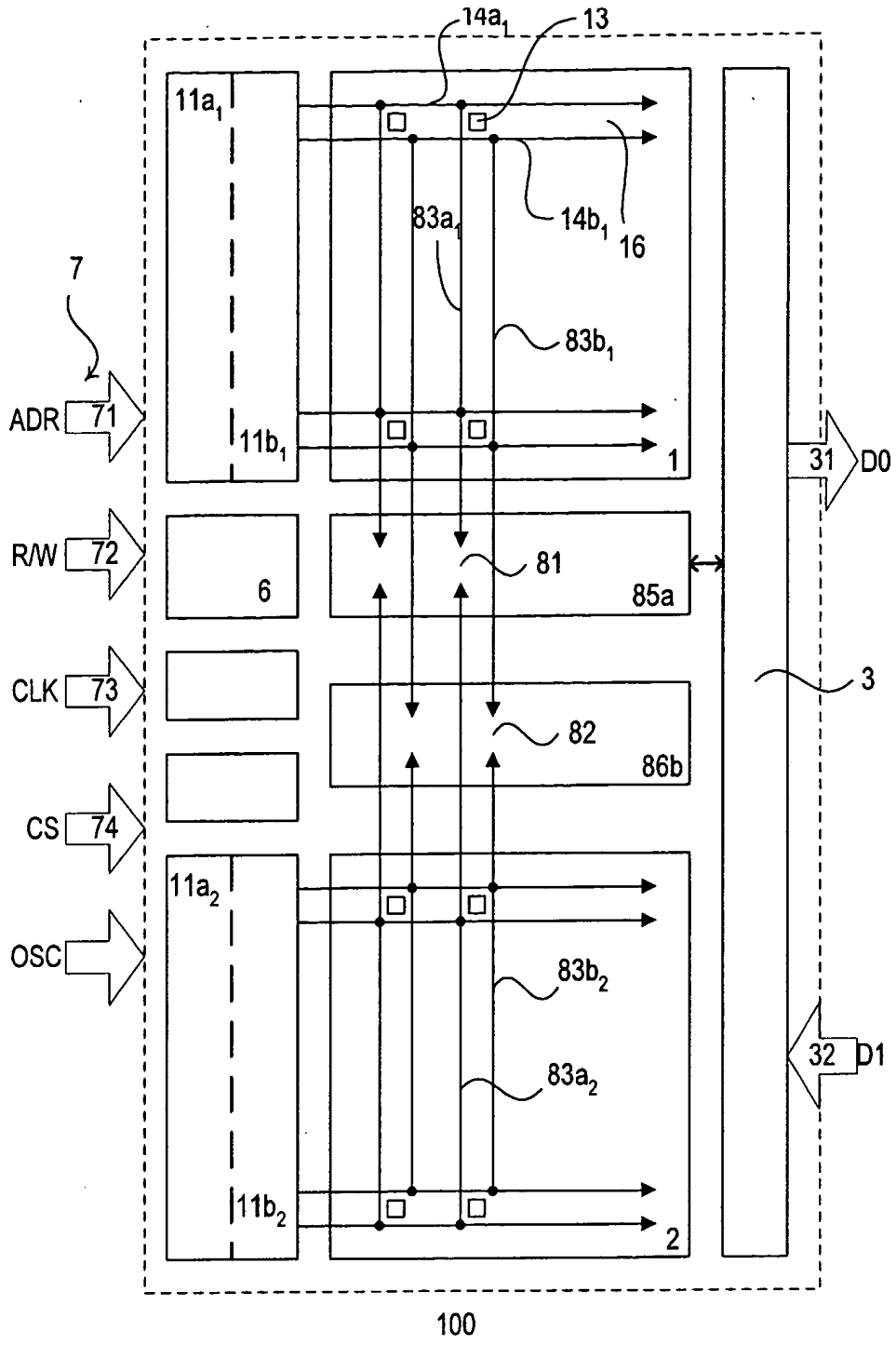
14a1
13
11a1
83a1
14b1
16
7
83b1
ADR
71
11b1
1
31
D0
R/W
72
6
81
85a
CLK
73
3
82
86b
CS
74
11a2
OSC
83b2
32
D1
83a2
11b2
2
100

FIG 1

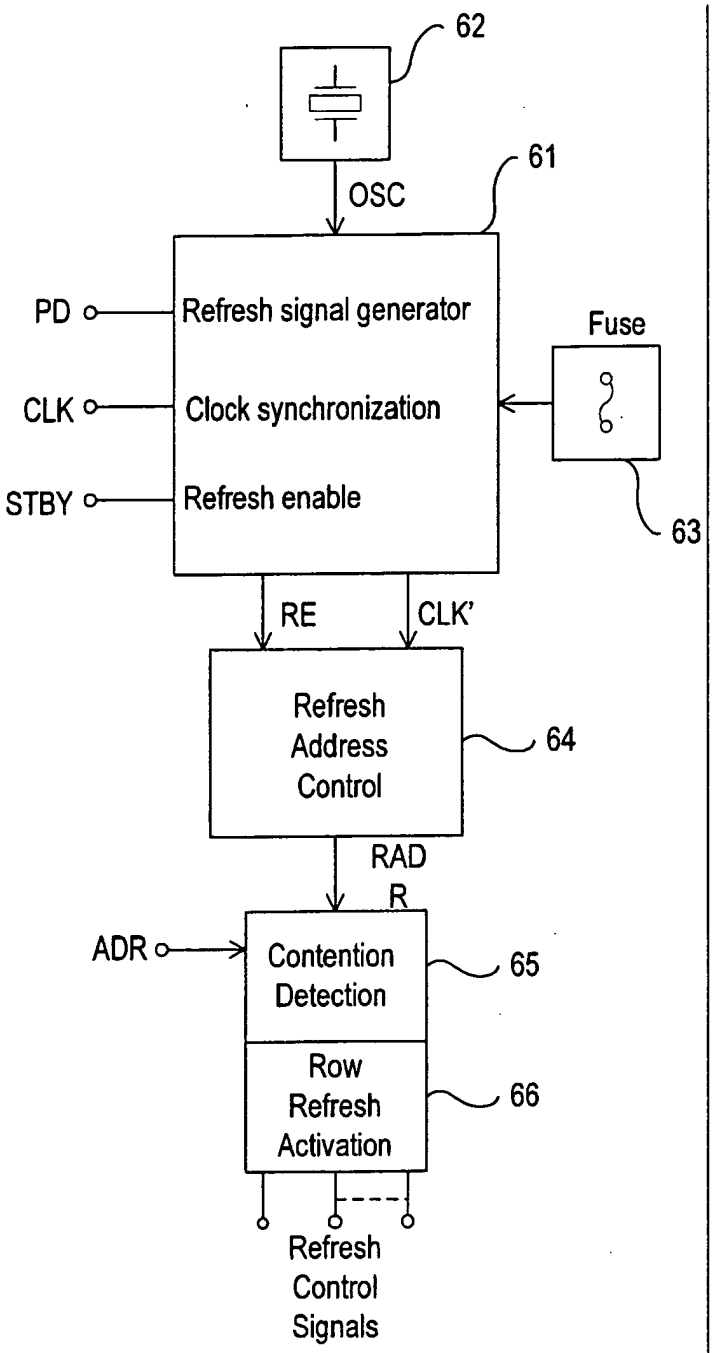
62
61
OSC
PD
Refresh signal generator
Fuse
CLK
Clock synchronization
STBY
Refresh enable
63
RE
CLK'
Refresh
Address
Control
64
RAD
R
ADR
Contention
Detection
65
Row
Refresh
Activation
66
Refresh
Control
Signals

FIG 2

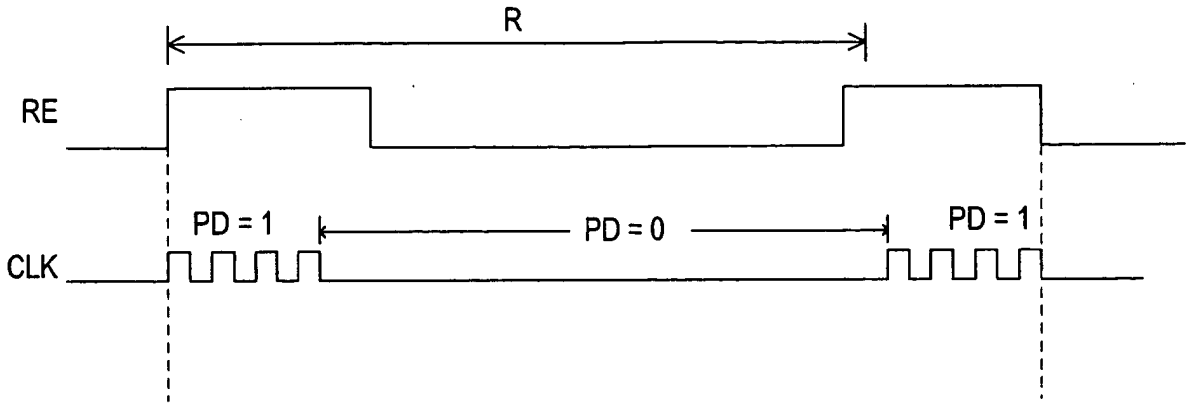

FIG 3

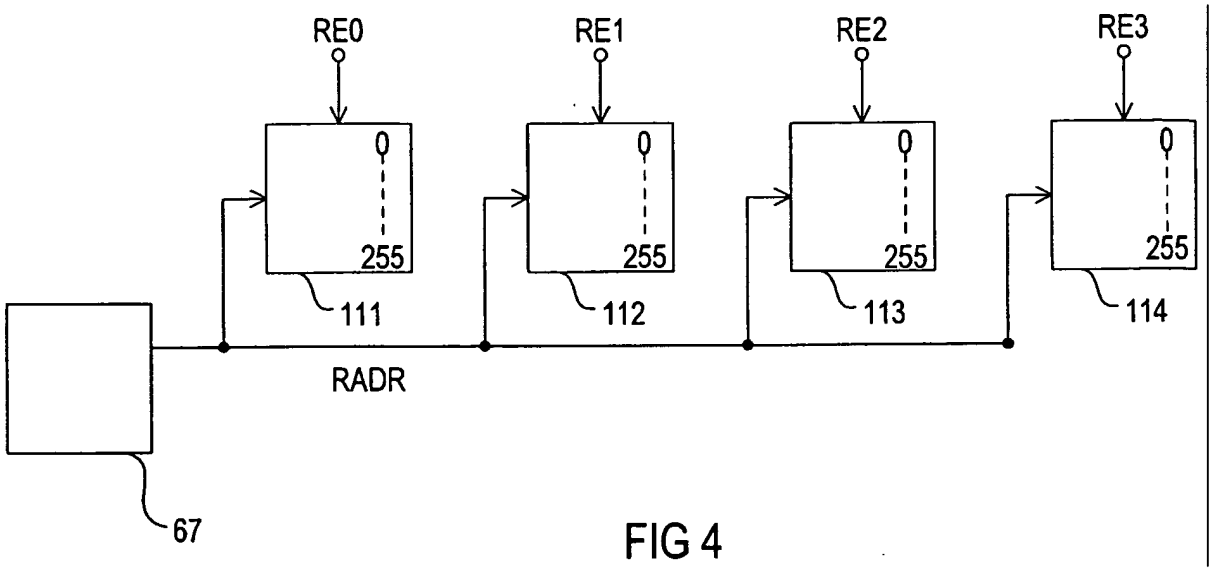

FIG 4

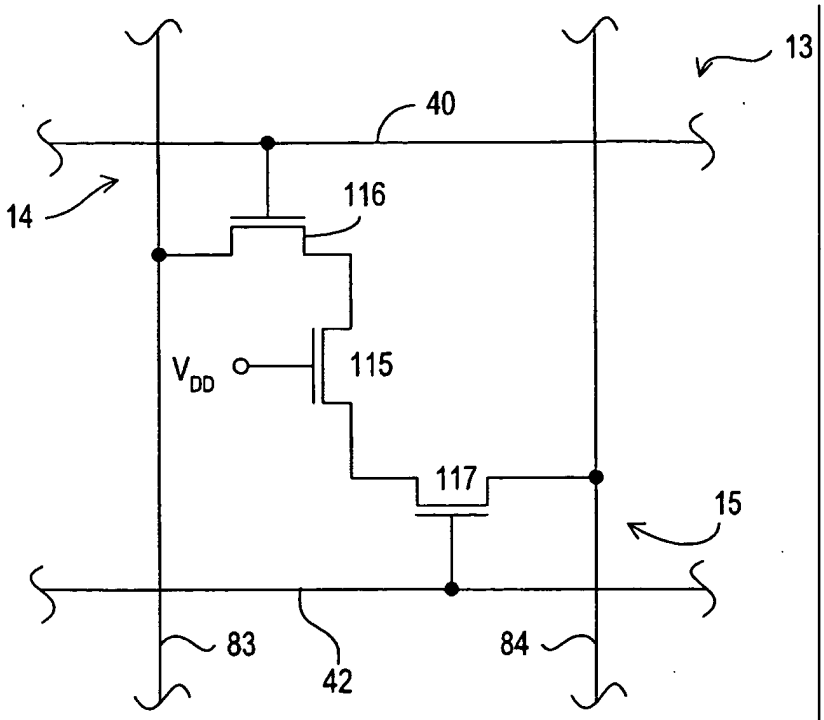

FIG 5